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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	40

Application Number	09/360,069
Filing Date	07/23/1999
First Named Inventor	Peter Wohl
Art Unit	2123
Examiner Name	Eduardo Garcia Otero
Attorney Docket Number	SYN-0136(RCE)

ENCLOSURES *(check all that apply)*

- ☒ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Terminal Disclaimer
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Statement Under 37 CFR 3.73(b)
- ☐ CD, Number of CD(s) _____
- ☐ Request for Refund

Remarks

- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☒ Appeal Communication to TC *(Appeal Notice, Brief, Reply Brief)*
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) *(please identify below):*

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SIGNATURE OF APPLICANT, ATTORNEY OR AGENT

Firm Name	BEVER, HOFFMAN & HARMS, LLP	Customer Number	35273
Signature			
Printed Name	Jeanette S. Harms		
Date	January 24, 2005	Reg. No.	35,537

CERTIFICATE OF TRANSMISSION/MAILING

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Signature	Rebecca A Baumann		
Typed or printed name	Rebecca A. Baumann	Date	January 24, 2005

PTO/SB/17 (12-04)
Approved for use through 07/31/2006. OMV 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Effective on 12/08/2004
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818)

FEE TRANSMITTAL For FY 2005

☐ Applicant claims small entity status. See 37 C.F.R. § 1.27

TOTAL AMOUNT OF PAYMENT | **($) 500.00**

Complete if Known	
Application Number	09/360,069
Filing Date	07/23/1999
First Named Inventor	Peter Wohl
Examiner Name	Eduardo Garcia Otero
Art Unit	2123
Attorney Docket No	SYN-0136(RCE)

METHOD OF PAYMENT (check all that apply)

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☒ Deposit Account Deposit Account Number: **50-0574** Deposit Account Name: **Bever, Hoffman & Harms, LLP**

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	**Fees Paid ($)**
Utility	300	150	500	250	200	100	$
Design	200	100	100	50	130	65	$
Plant	200	100	300	150	160	80	$
Reissue	300	150	500	250	600	300	$
Provisional	200	100	0	0	0	100	$

2. EXCESS CLAIM FEES

Fee Description	Fee($)	Small Entity Fee($)
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee($)	**Fee Paid ($)**	Multiple Dependent Claims		
	- 20 or HP =	x	=		Fee($)	Fee($)

HP = highest number of total claims paid for, if great than 20

Indep. Claims	Extra Claims	Fee($)	**Fee Paid ($)**
	- 3 or HP =	x	=

HP = highest number of total claims paid for, if great than 3

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 USC 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee($)	Fee Paid ($)
- 100 =	5- = (round up to a whole number)	x	=	

4. OTHER FEE(S)

	Fee Paid ($)
Non-English Specification - $130 fee (no small entity discount)	____
Other: **Appeal Brief**	**$500.00**

SUBMITTED BY

Signature:	Registration No.	35,537	Telephone: (408) 451-5907
Name (Print/Type) Jeanette S. Harms			Date: January 24, 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Peter Wohl et al.

Assignee: Synopsys, Inc.

Title: METHOD AND SYSTEM FOR GENERATING AN ATPG MODEL OF A MEMORY FROM BEHAVIORAL DESCRIPTIONS

Serial No.: 09/360,069 File Date: July 23, 1999

Examiner: Eduardo Garcia-Otero Art Unit: 2123

Docket No.: SYN-0136(RCE)

Date: January 24, 2005

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Sir:

This Appeal Brief, filed in triplicate, is in support of the Notice of Appeal dated December 27, 2004.

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INDEX

I. REAL PARTY IN INTEREST

The real party in interest is the assignee, Synopsys, Inc., pursuant to the Assignment recorded in the U.S. Patent and Trademark Office on July 23, 1999 on Reel 010132, Frame 0971.

II. RELATED APPEALS AND INTERFERENCES

Based on information and belief, there are no other appeals or interferences that could directly affect or be directly affected by or have a bearing on the decision by the Board of Patent Appeals in the pending appeal.

III. STATUS OF CLAIMS

Claims 37-53 and 55-58 are pending. Claims 1-36 and 54 are cancelled. Claims 37-53 and 55-58 stand rejected.

In the present paper, rejected Claims 37-53 and 55-58 are appealed.

Pending Claims 37-53 and 55-58 are listed in Appendix A.

IV. STATUS OF AMENDMENTS

Claims 37, 38, 40, 42, 45, 47, 48, 49, 50, 51, 52, 53, and 55 were amended in this RCE application prior to a final rejection.

V. SUMMARY OF THE INVENTION

The present invention is directed to electronic design automation (EDA). In particular, the invention is directed to memory models compatible with a simulation tool and an automatic test pattern generation (ATPG) tool. Advantageously, this memory model includes a plurality of primitives, wherein each primitive representing a defined functionality of a memory.

For example, Figure 6A (shown below) illustrates an exemplary ATPG memory model that can be generated from a behavioral description using an ATPG memory model generation process. As described in the Specification on page 18, lines 16-25, ATPG memory model 650 represents a structural model of a RAM described by a behavioral description. As shown in Figure 6A, ATPG memory model 650 includes a memory primitive 1100, an address bus primitive 1140, a data bus primitive 1130, a read port primitive 1140, and a plurality of memory output primitives 1150. The Specification on page 19, lines 1-13, describes the primitive connections shown in Figure 6A.

Advantageously, these primitives closely model the functionality of the RAM described by the behavioral description. Therefore, in an ATPG model generation process, each primitive (i.e. memory primitive 1100, address bus primitive 1140, data bus primitive 1130, read port primitive 1140, and the memory output primitives 1150) can be configured. Specification, page 20, line 4 to page 21, line 24. After the ATPG primitives are configured, the ATPG memory model can be used for test pattern generation. Specification, page 21, line 26 to page 22, line 2.

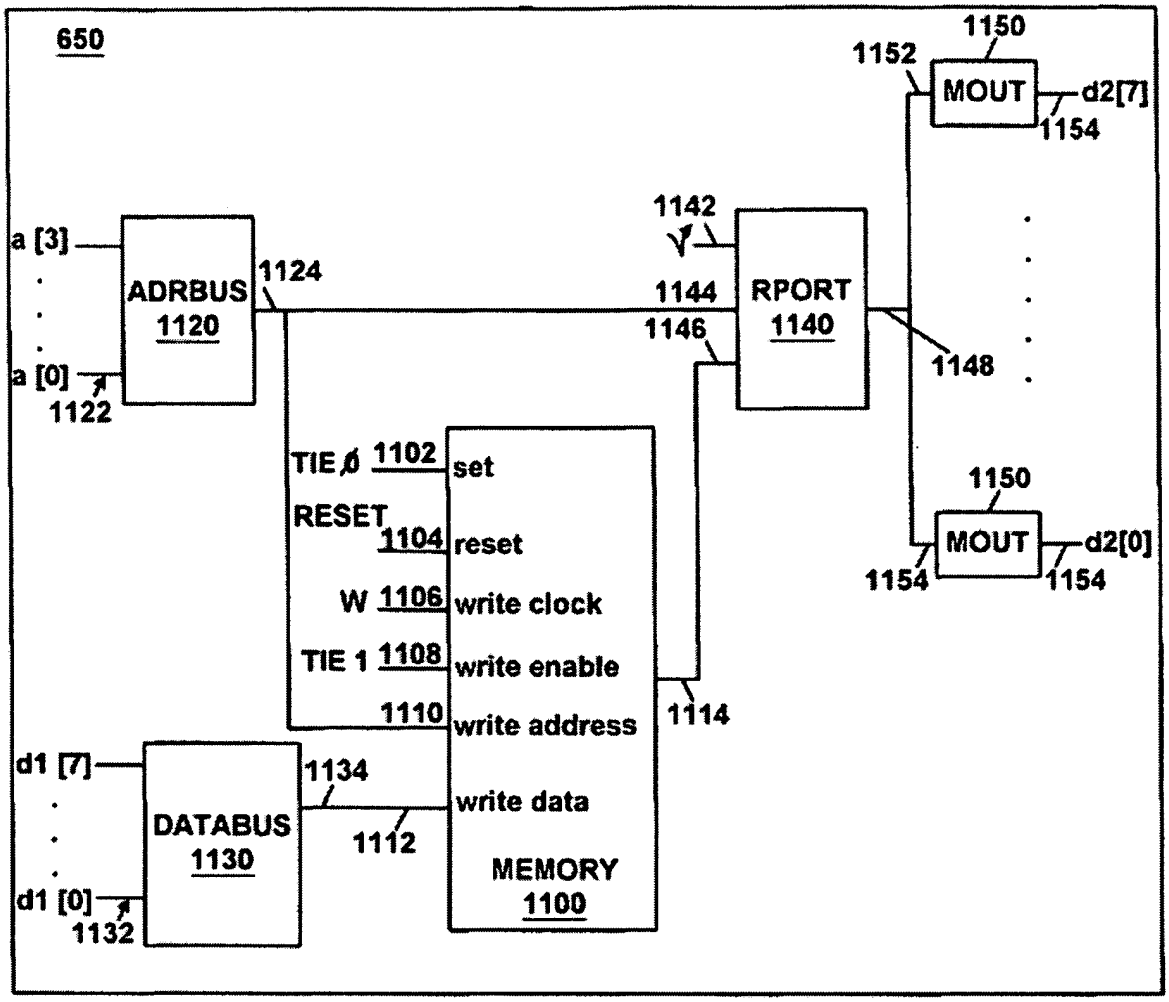

650
1150
1152
MOUT
d2[7]
1154
1142
a [3]
ADRBUS
1120
1124
1144
RPORT
1140
1146
1148
a [0]
1122
TIE 0 1102
set
RESET
1104
reset
1150
MOUT
d2[0]
1154
1154
W 1106
write clock
TIE 1 1108
write enable
1110
write address
1114
d1 [7]
1134
write data
DATABUS
1130
1112
MEMORY
1100
d1 [0]
1132

FIGURE 6A

In another example, Figure 10 (shown below) illustrates a combined content addressable memory (CAM) and random access memory (RAM) model 1000 usable for simulation and automatic test pattern generation. CAM-RAM model 1000 can include a first memory primitive 1100a, a data bus primitive (see Figure 11C, also shown below)(for coupling to line 1164), a compare port primitive 1160, a first plurality of memory output primitives 1150a-f, an address bus primitive 1120, a second memory primitive 1100b, a read data port primitive 1140, and a second plurality of memory output primitives 1150g-n. The Specification on page 34, line 25 to page 35, line 12 describes the primitive connections shown in Figure 10.

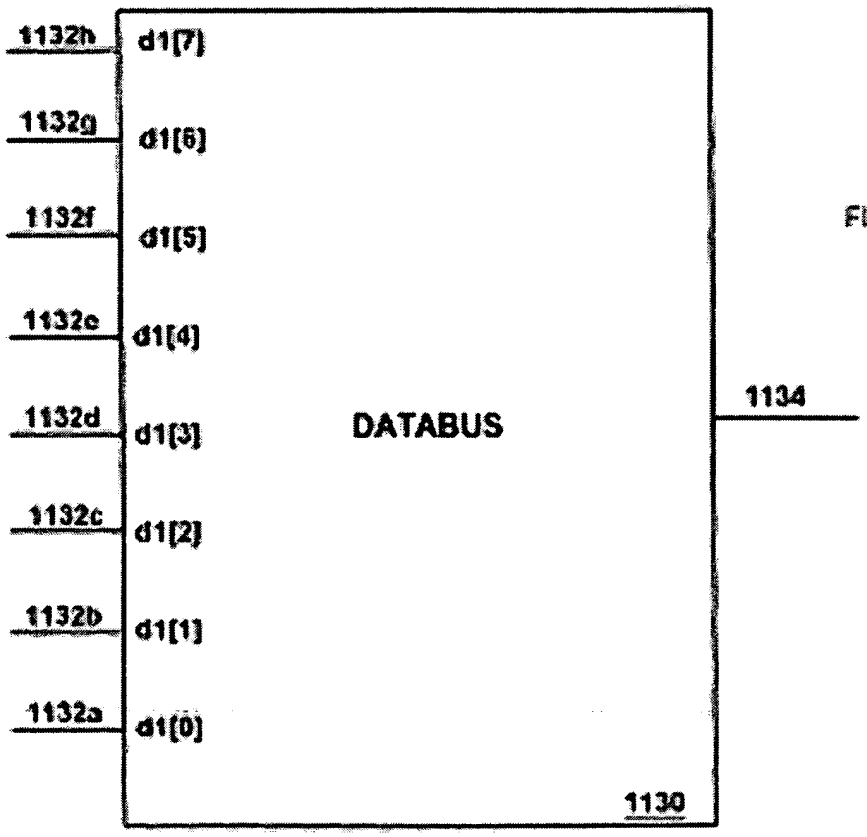


FIGURE 11C

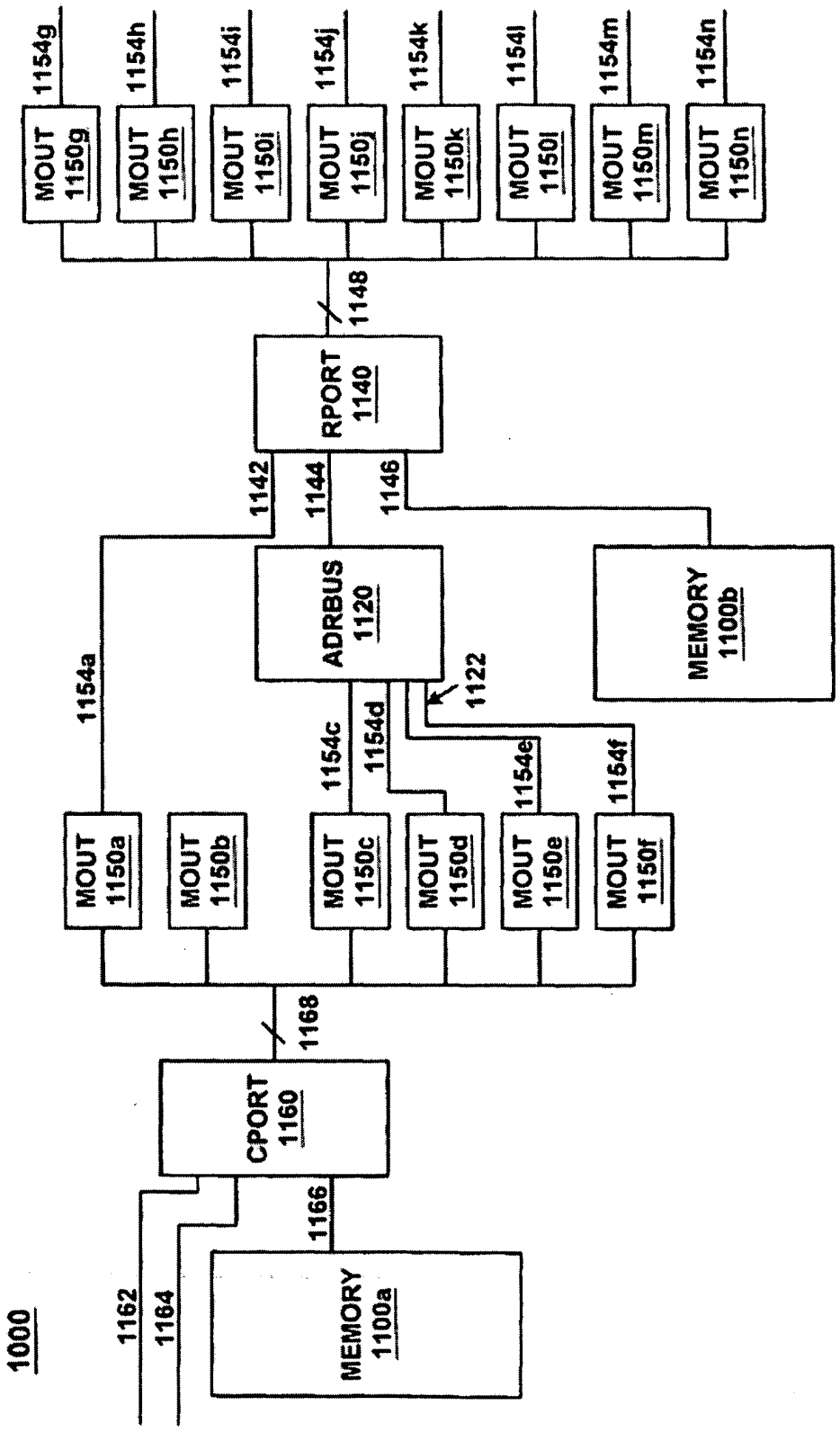

1000
MEMORY 1100a
1162
1164
1166
CPORT 1160
1168
MOUT 1150a
MOUT 1150b
MOUT 1150c
MOUT 1150d
MOUT 1150e
MOUT 1150f
MOUT 1150g
MOUT 1150h
MOUT 1150i
MOUT 1150j
MOUT 1150k
MOUT 1150l
MOUT 1150m
MOUT 1150n
1154a
1154c
1154d
1154e
1154f
1154g
1154h
1154i
1154j
1154k
1154l
1154m
1154n
ADRBUS 1120
1122
RPORT 1140
1142
1144
1146
1148
MEMORY 1100b

FIGURE 10

VI. ISSUES

The following issue is presented to the Board of Appeals for decision:

(A) Whether Claims 37-47, 49, 51-53, and 55-58 are patentable under 35 U.S.C. 102(b) over U.S. Patent 5,696,771 (Beausang)

(B) Whether Claims 48 and 50 are patentable under 35 U.S.C. 103(a) over U.S. Patent 5,696,771 (Beausang) in view of "Testing Untestable Faults In Three-State Circuits" by Wohl et al., published in 1996, IEEE pages 324-333 (Testing).

VII. GROUPING OF THE CLAIMS

Claims 37-53 stand or fall together. Claims 37-53 are directed to specific embodiments of memory models including primitives and their interconnections.

Claims 55-58 stand or fall together. Claims 55-58 are directed to the use of primitives to form a memory model, i.e. these claims are at a much more conceptual level than Claims 37-53.

Therefore, Appellant believes that Claims 37-53 and 55-58 are separately patentable.

VIII. ARGUMENTS

A. Claims 37-47, 49, 51-53, and 55-58 are patentable under 35 U.S.C. 102(b) over U.S. Patent 5,696,771 (Beausang)

Claim 37 Is Patentable Over Beausang

Claim 37 recites:

A memory model usable for simulation and automatic test pattern generation, the memory model comprising:

a memory primitive comprising a write_address port, a write_data port, and an output port;

a read data port primitive comprising a read_data port for coupling to the output port of the memory primitive, a read_address port, and an output port;

an address bus primitive comprising an output port for coupling to the write_address port of the memory primitive and the read_address port of the read data port primitive;

a data bus primitive comprising an output port for coupling to the write_data port of the memory primitive; and

a plurality of memory out primitives, each memory out primitive comprising an input port for coupling to the output port of the read data port primitive.

The Office Action cites Beausang at col. 1, lines 42-67, col. 14, line 40, element 230 of Fig. 1, elements 605 and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the elements of Claim 37. Applicants will now address the inapplicability of each citation to Claim 37.

Col. 1, lines 42-67 of Beausang states:

The behavior levels and RTL levels consist generally of descriptions of the circuit expressed with program-like constructs, such as variables, operators conditional loops, procedures and functions. At the logic level, the descriptions of the circuit are expressed with Boolean equations. The HDL can be used along with a set of circuit constraints as an input to a computer implemented compiler (also called a "silicon compiler"). The computer implemented compiler program processes this description of the integrated circuit and generates therefrom a detailed list of logic components and the interconnections between these components. This list is called a "netlist." The components of a netlist can include primitive cells such as full-

> adders, NAND gates, NOR gates, XOR gates, latches, and D-flip flops, etc. and their interconnections used to form a custom design.
>
> In processing the HDL input, the compiler first generates a netlist of generic primitive cells that are technology independent. The compiler then applies a particular cell library to this generic netlist (this process is called mapping) in order to generate a technology dependent mapped netlist. The mapping process converts the logical representation which is independent of technology into a form which is technology dependent. The mapped netlist has recourse to standard circuits, or cells which are available within a cell library forming a part of the data available to the computer system.

This citation of Beausang teaches nothing regarding the memory model recited in Claim 37. Specifically, the above citation to Beausang teaches nothing regarding a memory primitive comprising a write_address port, a write_data port, and an output port, nor a read data port primitive comprising a read_data port for coupling to the output port of the memory primitive, a read_address port, and an output port, nor an address bus primitive comprising an output port for coupling to the write_address port of the memory primitive and the read_address port of the read data port primitive, nor a data bus primitive comprising an output port for coupling to the write_data port of the memory primitive, nor a plurality of memory out primitives, each memory out primitive comprising an input port for coupling to the output port of the read data port primitive. Beausang's generalized statement (and the definitions of "primitive" provided by the McGraw-Hill Dictionary and the MS Dictionary) regarding primitive cells does not disclose the primitives recited by Applicants. Moreover, the primitives of Beausang are used to model logic, not memory as recited by Applicants.

In short, col. 1, lines 42-67 of Beausang fails to teach any limitation of Claim 37. Applicants further note the characterization in the Office Action that "and their interconnections" discloses the recited address bus and data bus primitives is incorrect and not supported. Applicants note that the generic term "interconnections" teaches nothing regarding what and how such interconnections are made, which is a notable aspect of Applicants' model.

Col. 14, lines 39-42 (providing the context for line 40) of Beausang states:

> Technology independent netlist 620 is composed of logical primitives and operators of the IC layout but the components described therein contain no structure.

This citation fails to teach anything regarding the memory model recited in Claim 37, much less the recited primitives comprising the memory model and their interconnections.

Element 230 of Fig. 1 in Beausang refers to a technology dependent cell library. Col. 2, line 50. Cell library 230 contains specific information selected such as the cell logic, number of gates, area consumption, power consumption, pin descriptions, etc., for each cell in the library 230. Col. 2, lines 51-55. Element 230 fails to teach anything regarding the memory model recited in Claim 37, much less the recited primitives comprising the memory model and their interconnections.

Elements 605 of Fig. 8 in Beausang refers to an HDL description that can be of a number of different formats, such as VHDL or Verilog and can also represent an entire IC design, but typically represents a module of the overall IC design. Col. 14, lines 27-30. Element 605 fails to teach anything regarding the memory model recited in Claim 37, much less the

recited primitives comprising the memory model and their interconnections.

Element 655 of Fig. 8 in Beausang refers to using a combinational ATPG process to generate test vectors. Col. 16, lines 16-18. Block 655 can also perform ATPG formatting in which test vectors generated by the ATPG processes are altered or modified so that they will operate with particular specified set of test equipment that accepts a particular format as input. Col. 16, lines 19-23. Element 655 fails to teach anything regarding the memory model recited in Claim 37, much less the recited primitives comprising the memory model and their interconnections.

Element 660 of Fig. 8 in Beausang refers to test vectors that can be loaded into the result IC chip to check for faults within the chip. Col. 16, lines 26-28. Element 660 fails to teach anything regarding the memory model recited in Claim 37, much less the recited primitives comprising the memory model and their interconnections.

Element 790 of Fig. 9 in Beausang refers to a logic block in which the TR compiler 625 performs logic verification to determine if the design generated by logic block 785 and the HDL design input at logic block 710 are functionally equivalent. Col. 20, lines 3-6. Element 790 fails to teach anything regarding the memory model recited in Claim 37, much less the recited primitives comprising the memory model and their interconnections.

Because Beausang fails to disclose or suggest the recited limitations of Claim 37, Applicants request reconsideration and withdrawal of the rejection of Claim 37.

Claim 38 Is Patentable Over Beausang

Claim 38 recites:

> The memory model of Claim 37, wherein the memory primitive further includes:
> a set input port;
> á reset port;
> a write_clock port; and
> a write_enable port.

Claim 38 depends from Claim 37 and therefore is patentable for at least the reasons presented for Claim 37. Based on those reasons, Applicants request reconsideration and withdrawal of the rejection of Claim 38.

Claim 39 Is Patentable Over Beausang

Claim 39 recites:

> The memory model of Claim 37, wherein the read data port primitive represents a read port functionality of the memory.

Claim 39 depends from Claim 37 and therefore is patentable for at least the reasons presented for Claim 37. The Office Action cites Beausang at col. 1, lines 53-67, col. 14, line 40, element 230 of Fig. 1, elements 605, 655, and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the elements of Claim 39 (the same citations used for Claim 37). Applicants have addressed the inapplicability of each citation to Claim 37. Claim 39 recites further limitations regarding the read data port primitive. Because Beausang fails to disclose or suggest a read data port primitive, Beausang logically cannot disclose a further limitation regarding that primitive. Therefore, Applicants request reconsideration and withdrawal of the rejection of Claim 39.

Claim 40 Is Patentable Over Beausang

Claim 40 recites:

> The memory model of Claim 39, wherein a dimension of the output port of the read data port corresponds to a data dimension of the memory primitive.

Claim 40 depends from Claim 39 and therefore is patentable for at least the reasons presented for Claim 39. The Office Action cites Beausang at col. 1, lines 53-67, col. 14, line 40, element 230 of Fig. 1, elements 605, 655, and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the elements of Claim 40 (the same citations used for Claim 37). Because Beausang fails to disclose or suggest a read data port, Beausang logically cannot disclose a further limitation regarding that port. Therefore, Applicants request reconsideration and withdrawal of the rejection of Claim 40.

Claim 41 Is Patentable Over Beausang

Claim 41 recites:

> The memory model of Claim 37, wherein the address bus primitive represents an address functionality of a memory.

Claim 41 depends from Claim 37 and therefore is patentable for at least the reasons presented for Claim 37. The Office Action cites Beausang at col. 1, lines 53-67, col. 14, line 40, element 230 of Fig. 1, elements 605, 655, and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the elements of Claim 41 (the same citations used for Claim 37). Applicants have addressed the inapplicability of each citation to Claim 37. Claim 41 recites a further limitation regarding the address bus primitive. Because Beausang fails to disclose or suggest an address bus primitive, Beausang logically cannot disclose a further limitation regarding that primitive. Therefore,

Applicants request reconsideration and withdrawal of the rejection of Claim 41.

Claim 42 Is Patentable Over Beausang

Claim 42 recites:

> The memory model of Claim 41, wherein the address bus primitive includes:
> a plurality of input ports corresponding to an address dimension of the memory primitive.

Claim 42 depends from Claim 41 and therefore is patentable for at least the reasons presented for Claim 41. The Office Action cites Beausang at col. 1, lines 53-67, col. 14, line 40, element 230 of Fig. 1, elements 605, 655, and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the elements of Claim 42 (the same citations used for Claim 37). Because Beausang fails to disclose or suggest an address bus primitive, Beausang logically cannot disclose a further limitation regarding that primitive. Therefore, Applicants request reconsideration and withdrawal of the rejection of Claim 42.

Claim 43 Is Patentable Over Beausang

Claim 43 recites:

> The memory model of Claim 42, wherein the address bus primitive further includes an attribute indicating whether an incoming address is encoded or decoded.

Claim 43 depends from Claim 42 and therefore is patentable for at least the reasons presented for Claim 42. The Office Action cites Beausang at col. 1, lines 53-67, col. 14, line 40, element 230 of Fig. 1, elements 605, 655, and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the elements of Claim 38 (the same citations used for Claim 37). Because Beausang fails to disclose or suggest an address bus primitive, Beausang

logically cannot disclose a further limitation regarding that primitive. Therefore, Applicants request reconsideration and withdrawal of the rejection of Claim 43.

Claim 44 Is Patentable Over Beausang

Claim 44 recites:

> The memory model of Claim 43, wherein the data bus primitive represents a data bus functionality of the memory.

Claim 44 depends from Claim 43 and therefore is patentable for at least the reasons presented for Claim 43. The Office Action cites Beausang at col. 1, lines 53-67, col. 14, line 40, element 230 of Fig. 1, elements 605, 655, and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the elements of Claim 44 (the same citations used for Claim 37). Because Beausang fails to disclose or suggest a data bus primitive, Beausang logically cannot disclose a further limitation regarding that primitive. Therefore, Applicants request reconsideration and withdrawal of the rejection of Claim 44.

Claim 45 Is Patentable Over Beausang

Claim 45 recites:

> The memory model of Claim 44, wherein the data bus includes:
> a plurality of input ports corresponding to a data dimension of the memory primitive.

Claim 45 depends from Claim 44 and therefore is patentable for at least the reasons presented for Claim 44. The Office Action cites Beausang at col. 1, lines 53-67, col. 14, line 40, element 230 of Fig. 1, elements 605, 655, and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the elements of Claim 45 (the same citations used for Claim 37). Because Beausang fails

to disclose or suggest a data bus primitive, Beausang logically cannot disclose a further limitation regarding that primitive. Therefore, Applicants request reconsideration and withdrawal of the rejection of Claim 45.

Claim 46 Is Patentable Over Beausang

Claim 46 recites:

> The memory model of Claim 37, wherein each memory out primitive represents a simulated value storage functionality of the memory.

Claim 46 depends from Claim 37 and therefore is patentable for at least the reasons presented for Claim 37. The Office Action cites Beausang at col. 1, lines 53-67, col. 14, line 40, element 230 of Fig. 1, elements 605, 655, and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the elements of Claim 46 (the same citations used for Claim 37). Applicants have addressed the inapplicability of each citation to Claim 37. Claim 46 recites a further limitation regarding the memory out primitive. Because Beausang fails to disclose or suggest a memory out primitive, Beausang logically cannot disclose a further limitation regarding that primitive. Therefore, Applicants request reconsideration and withdrawal of the rejection of Claim 46.

Claim 47 Is Patentable Over Beausang

Claim 47 recites:

> The memory model of Claim 37, wherein each memory out primitive includes an output port.

Claim 47 depends from Claim 37 and therefore is patentable for at least the reasons presented for Claim 37. The Office Action cites Beausang at col. 1, lines 53-67, col. 14, line 40, element 230 of Fig. 1, elements 605, 655, and 660 of Fig. 8, and

element 790 of Fig. 9 as disclosing the elements of Claim 47 (the same citations used for Claim 37). Applicants have addressed the inapplicability of each citation to Claim 37. Claim 47 recites a further limitation regarding the memory out primitive. Because Beausang fails to disclose or suggest a memory out primitive, Beausang logically cannot disclose a further limitation regarding that primitive. Therefore, Applicants request reconsideration and withdrawal of the rejection of Claim 47.

Claim 49 Is Patentable Over Beausang

Claim 49 recites:

> The memory model of Claim 47, wherein a plurality of edge-triggered registers can be coupled to the output ports of the memory out primitives, thereby representing an attribute of the read data port primitive.

Claim 49 depends from Claim 47 and therefore is patentable for at least the reasons presented for Claim 47. The Office Action cites Beausang at col. 1, lines 53-67, col. 14, line 40, element 230 of Fig. 1, elements 605, 655, and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the elements of Claim 38 (the same citations used for Claim 37). Because Beausang fails to disclose or suggest a memory out primitive or a read data port primitive, Beausang logically cannot disclose a further limitation that a plurality of edge-triggered registers can be coupled to the output ports of the memory out primitives, thereby representing an attribute of the read data port primitive. Therefore, Applicants request reconsideration and withdrawal of the rejection of Claim 49.

Claim 51 Is Patentable Over Beausang

Claim 51 recites:

> A content addressable memory model usable for simulation and automatic test pattern generation, the content addressable memory model comprising:
>
> a memory primitive including an output port;
>
> a compare port primitive including a data port for coupling to the output port of the memory primitive, a data bus port, and an output port;
>
> a data bus primitive including an output port for coupling to the data bus port of the compare port primitive;
>
> a plurality of memory output primitives, each memory output primitive including an input port for coupling to the output port of the compare port primitive and an output port; and
>
> an address bus primitive including input ports for coupling the output ports of a set of the memory output primitives.

The Office Action cites Beausang at col. 1, lines 53-67, col. 14, line 40, element 230 of Fig. 1, elements 605, 655, and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the elements of Claim 37. Applicants will now address the inapplicability of each citation to Claim 51.

Col. 1, lines 53-67 of Beausang states:

> The components of a netlist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates, latches, and D- flip flops, etc. and their interconnections used to form a custom design.
>
> In processing the HDL input, the compiler first generates a netlist of generic primitive cells that are technology independent. The compiler then applies a particular cell library to this generic netlist (this process is called mapping) in order to generate a technology dependent mapped netlist. The mapping process converts the logical representation which is independent of technology into a form which is technology dependent. The mapped netlist has

> recourse to standard circuits, or cells which are available within a cell library forming a part of the data available to the computer system.

This citation of Beausang teaches nothing regarding the content addressable memory model recited in Claim 51. Specifically, the above citation to Beausang teaches nothing regarding a memory primitive including an output port, nor a compare port primitive including a data port for coupling to the output port of the memory primitive, a data bus port, and an output port, nor a data bus primitive including an output port for coupling to the data bus port of the compare port primitive, nor a plurality of memory output primitives, each memory output primitive including an input port for coupling to the output port of the compare port primitive and an output port, nor an address bus primitive including input ports for coupling the output ports of a set of the memory output primitives. In short, col. 1, lines 53-67 of Beausang fails to teach any limitation of Claim 51. Beausang's generalized statement regarding primitive cells does not disclose the primitives recited by Applicants. Moreover, the primitives of Beausang are used to model logic, not memory as recited by Applicants.

Col. 14, lines 39-42 (providing the context for line 40) of Beausang states:

> Technology independent netlist 620 is composed of logical primitives and operators of the IC layout but the components described therein contain no structure.

This citation fails to teach anything regarding the content addressable memory model recited in Claim 51, much less the recited primitives comprising the content addressable memory model and their interconnections.

Element 230 of Fig. 1 in Beausang refers to a technology dependent cell library. Col. 2, line 50. Cell library 230

contains specific information selected such as the cell logic, number of gates, area consumption, power consumption, pin descriptions, etc., for each cell in the library 230. Col. 2, lines 51-55. Element 230 fails to teach anything regarding the content addressable memory model recited in Claim 51, much less the recited primitives comprising the content addressable memory model and their interconnections.

Elements 605 of Fig. 8 in Beausang refers to an HDL description that can be of a number of different formats, such as VHDL or Verilog and can also represent an entire IC design, but typically represents a module of the overall IC design. Col. 14, lines 27-30. Element 605 fails to teach anything regarding the content addressable memory model recited in Claim 51, much less the recited primitives comprising the content addressable memory model and their interconnections.

Element 655 of Fig. 8 in Beausang refers to using a combinational ATPG process to generate test vectors. Col. 16, lines 16-18. Block 655 can also perform ATPG formatting in which test vectors generated by the ATPG processes are altered or modified so that they will operate with particular specified set of test equipment that accepts a particular format as input. Col. 16, lines 19-23. Element 655 fails to teach anything regarding the content addressable memory model recited in Claim 51, much less the recited primitives comprising the content addressable memory model and their interconnections.

Element 660 of Fig. 8 in Beausang refers to test vectors that can be loaded into the result IC chip to check for faults within the chip. Col. 16, lines 26-28. Element 660 fails to teach anything regarding the content addressable memory model recited in Claim 51, much less the recited primitives comprising the content addressable memory model and their interconnections.

Element 790 of Fig. 9 in Beausang refers to a logic block in which the TR compiler 625 performs logic verification to determine if the design generated by logic block 785 and the HDL design input at logic block 710 are functionally equivalent. Col. 20, lines 3-6. Element 790 fails to teach anything regarding the content addressable memory model recited in Claim 51, much less the recited primitives comprising the content addressable memory model and their interconnections.

Because Beausang fails to disclose or suggest the recited limitations of Claim 51, Applicants request reconsideration and withdrawal of the rejection of Claim 51.

Claim 52 Is Patentable Over Beausang

Claim 52 recites:

> The content addressable memory model of Claim 51, wherein the compare port primitive further includes:
>
> a compare enable port for receiving a compare signal.

Claim 52 depends from Claim 51 and therefore is patentable for at least the reasons presented for Claim 51. The Office Action cites Beausang at col. 1, lines 53-67, col. 14, line 40, element 230 of Fig. 1, elements 605, 655, and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the elements of Claim 52 (the same citations used for Claim 51). Applicants have addressed the inapplicability of each citation to Claim 51. Claim 52 recites a further limitation regarding the compare port primitive. Because Beausang fails to disclose or suggest a compare port primitive, Beausang logically cannot disclose a further limitation regarding that primitive. Therefore, Applicants request reconsideration and withdrawal of the rejection of Claim 52.

Claim 53 Is Patentable Over Beausang

Claim 53 recites:

> A combined content addressable memory (CAM) and random access memory (RAM) model usable for simulation and automatic test pattern generation, the combined CAM and RAM model comprising:
> a first memory primitive including an output port;
> a data bus primitive including an output port;
> a compare port primitive for coupling to the memory primitive and the data bus primitive, the compare port primitive comprising;
> a compare enable port;
> a data bus port for coupling to the output port of the data bus primitive;
> a data port for coupling to the output port of the first memory primitive; and
> an output port;
> a first plurality of memory output primitives, each memory output primitive including an output port and an input port for coupling to the output port of the compare port primitive;
> an address bus primitive including an output port and input ports for coupling to output ports of a first subset of the first plurality of memory output primitives;
> a second memory primitive including an output port;
> a read data port primitive including a first input port for coupling to the output port of the second memory primitive, a second input port for coupling to an output port of the address bus primitive, and a third input port for coupling to the output ports of a second subset of the plurality of memory output primitives; and
> a second plurality of memory output primitives, each memory output primitive including an input port for coupling to an output port of the read data port primitive.

The Office Action cites Beausang at col. 1, lines 53-67, col. 14, line 40, element 230 of Fig. 1, elements 605, 655, and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the

elements of Claim 53. Applicants will now address the inapplicability of each citation to Claim 53.

Col. 1, lines 53-67 of Beausang states:

> The components of a netlist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates, latches, and D- flip flops, etc. and their interconnections used to form a custom design.
>
> In processing the HDL input, the compiler first generates a netlist of generic primitive cells that are technology independent. The compiler then applies a particular cell library to this generic netlist (this process is called mapping) in order to generate a technology dependent mapped netlist. The mapping process converts the logical representation which is independent of technology into a form which is technology dependent. The mapped netlist has recourse to standard circuits, or cells which are available within a cell library forming a part of the data available to the computer system.

This citation of Beausang teaches nothing regarding the combined CAM and RAM model recited in Claim 53. Specifically, the above citation to Beausang teaches nothing regarding a first memory primitive including an output port, nor a data bus primitive including an output port, nor a compare port primitive for coupling to the memory primitive and the data bus primitive, nor a compare port primitive comprising a compare enable port, a data bus port for coupling to the output port of the data bus primitive, a data port for coupling to the output port of the first memory primitive, and an output port, nor a first plurality of memory output primitives, each memory output primitive including an output port and an input port for coupling to the output port of the compare port primitive, nor an address bus primitive including an output port and input ports for coupling to output ports of a first subset of the first plurality of memory output primitives, nor a second memory

primitive including an output port, nor a read data port primitive including a first input port for coupling to the output port of the second memory primitive, a second input port for coupling to an output port of the address bus primitive, and a third input port for coupling to the output ports of a second subset of the plurality of memory output primitives, nor a second plurality of memory output primitives, each memory output primitive including an input port for coupling to an output port of the read data port primitive. In short, col. 1, lines 53-67 of Beausang fails to teach any limitation of Claim 53. Beausang's generalized statement regarding primitive cells does not disclose the primitives recited by Applicants. Moreover, the primitives of Beausang are used to model logic, not memory as recited by Applicants.

Col. 14, lines 39-42 (providing the context for line 40) of Beausang states:

> Technology independent netlist 620 is composed of logical primitives and operators of the IC layout but the components described therein contain no structure.

This citation fails to teach anything regarding the combined CAM and RAM model recited in Claim 53, much less the recited primitives comprising the combined CAM and RAM model and their interconnections.

Element 230 of Fig. 1 in Beausang refers to a technology dependent cell library. Col. 2, line 50. Cell library 230 contains specific information selected such as the cell logic, number of gates, area consumption, power consumption, pin descriptions, etc., for each cell in the library 230. Col. 2, lines 51-55. Element 230 fails to teach anything regarding the combined CAM and RAM model recited in Claim 53, much less the recited primitives comprising the combined CAM and RAM model and their interconnections.

Elements 605 of Fig. 8 in Beausang refers to an HDL description that can be of a number of different formats, such as VHDL or Verilog and can also represent an entire IC design, but typically represents a module of the overall IC design. Col. 14, lines 27-30. Element 605 fails to teach anything regarding the combined CAM and RAM model recited in Claim 53, much less the recited primitives comprising the combined CAM and RAM model and their interconnections.

Element 655 of Fig. 8 in Beausang refers to using a combinational ATPG process to generate test vectors. Col. 16, lines 16-18. Block 655 can also perform ATPG formatting in which test vectors generated by the ATPG processes are altered or modified so that they will operate with particular specified set of test equipment that accepts a particular format as input. Col. 16, lines 19-23. Element 655 fails to teach anything regarding the combined CAM and RAM model recited in Claim 53, much less the recited primitives comprising the combined CAM and RAM model and their interconnections.

Element 660 of Fig. 8 in Beausang refers to test vectors that can be loaded into the result IC chip to check for faults within the chip. Col. 16, lines 26-28. Element 660 fails to teach anything regarding the combined CAM and RAM model recited in Claim 53, much less the recited primitives comprising the combined CAM and RAM model and their interconnections.

Element 790 of Fig. 9 in Beausang refers to a logic block in which the TR compiler 625 performs logic verification to determine if the design generated by logic block 785 and the HDL design input at logic block 710 are functionally equivalent. Col. 20, lines 3-6. Element 790 fails to teach anything regarding the combined CAM and RAM model recited in Claim 53, much less the recited primitives comprising the combined CAM and RAM model and their interconnections.

Because Beausang fails to disclose or suggest the recited limitations of Claim 53, Applicants request reconsideration and withdrawal of the rejection of Claim 53.

Claim 55 Is Patentable Over Beausang

Claim 55 recites:

> A memory model compatible with a simulation tool and an automatic test pattern generation (ATPG) tool, the memory model including:
> a plurality of primitives, each primitive representing a defined functionality of a memory.

The Office Action cites Beausang at col. 1, lines 53-67, col. 14, line 40, element 230 of Fig. 1, elements 605, 655, and 660 of Fig. 8, and element 790 of Fig. 9 as disclosing the elements of Claim 55. Applicants will now address the inapplicability of each citation to Claim 55.

Col. 1, lines 53-67 of Beausang states:

> The components of a netlist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates, latches, and D- flip flops, etc. and their interconnections used to form a custom design.
> In processing the HDL input, the compiler first generates a netlist of generic primitive cells that are technology independent. The compiler then applies a particular cell library to this generic netlist (this process is called mapping) in order to generate a technology dependent mapped netlist. The mapping process converts the logical representation which is independent of technology into a form which is technology dependent. The mapped netlist has recourse to standard circuits, or cells which are available within a cell library forming a part of the data available to the computer system.

This citation of Beausang teaches nothing regarding the memory model including a plurality of primitives, wherein each primitive represents a defined functionality of a memory as

recited in Claim 55. Beausang's generalized statement regarding primitive cells does not disclose the memory model comprising multiple primitives recited by Applicants. Moreover, the primitives of Beausang are used to model logic, not memory as recited by Applicants.

Col. 14, lines 39-42 (providing the context for line 40) of Beausang states:

> Technology independent netlist 620 is composed of logical primitives and operators of the IC layout but the components described therein contain no structure.

This citation fails to teach anything regarding a memory model including a plurality of primitives, wherein each primitive represents a defined functionality of a memory.

Element 230 of Fig. 1 in Beausang refers to a technology dependent cell library. Col. 2, line 50. Cell library 230 contains specific information selected such as the cell logic, number of gates, area consumption, power consumption, pin descriptions, etc., for each cell in the library 230. Col. 2, lines 51-55. Element 230 fails to teach anything regarding a memory model including a plurality of primitives, wherein each primitive represents a defined functionality of a memory.

Elements 605 of Fig. 8 in Beausang refers to an HDL description that can be of a number of different formats, such as VHDL or Verilog and can also represent an entire IC design, but typically represents a module of the overall IC design. Col. 14, lines 27-30. Element 605 fails to teach anything regarding a memory model including a plurality of primitives, wherein each primitive represents a defined functionality of a memory.

Element 655 of Fig. 8 in Beausang refers to using a combinational ATPG process to generate test vectors. Col. 16, lines 16-18. Block 655 can also perform ATPG formatting in

which test vectors generated by the ATPG processes are altered or modified so that they will operate with particular specified set of test equipment that accepts a particular format as input. Col. 16, lines 19-23. Element 655 fails to teach anything regarding a memory model including a plurality of primitives, wherein each primitive represents a defined functionality of a memory.

Element 660 of Fig. 8 in Beausang refers to test vectors that can be loaded into the result IC chip to check for faults within the chip. Col. 16, lines 26-28. Element 660 fails to teach anything regarding a memory model including a plurality of primitives, wherein each primitive represents a defined functionality of a memory.

Element 790 of Fig. 9 in Beausang refers to a logic block in which the TR compiler 625 performs logic verification to determine if the design generated by logic block 785 and the HDL design input at logic block 710 are functionally equivalent. Col. 20, lines 3-6. Element 790 fails to teach anything regarding a memory model including a plurality of primitives, wherein each primitive represents a defined functionality of a memory.

Because Beausang fails to disclose or suggest the recited limitations of Claim 55, Applicants request reconsideration and withdrawal of the rejection of Claim 55.

Claims 56, 57, and 58 Are Patentable Over Beausang

Claim 56 depends from Claim 55 and therefore is patentable for at least the reasons presented for Claim 55. Claims 57 and 58 depend from Claim 56 and therefore are patentable for at least the reasons presented for Claim 56. Based on all of the above reasons, Applicants request reconsideration and withdrawal of the rejection of Claims 56, 57, and 58.

B. Claims 48 and 50 are patentable under 35 U.S.C. 103(a) over U.S. Patent 5,696,771 (Beausang) in view of "Testing Untestable Faults In Three-State Circuits" by Wohl et al., published in 1996, IEEE pages 324-333 (Testing).

The Combination Of Beausang and Testing Is Inappropriate

Beausang teaches a computer implemented process and system for determining a set of sequential cells within an IC design that can be scan replaced. Col. 4, lines 57-59. Specifically, Beausang teaches selecting sequential cells for scan replacement that offer best testability contribution and not selecting sequential scan cells for scan replacement that do not offer much testability contribution and/or are part of most critical paths within the design. Col. 4, lines 59-67.

Testing teaches how to use design particularities (such as bus keepers and resolving bus contention states to binary values) with transistor-level modeling and innovative use of ATPG methods to address test generation performance and test coverage problems generated by the extensive usage of tristate circuitry. Page 330-331 (Section 7. Summary).

Notably, the teaching of Testing does not help in determining the set of sequential cells within an IC design that can be scan replaced (Beausang). Nor does the teaching of Beausang help in determining an ATPG method to address test generation performance and test coverage problems generated by the use of tristate circuitry (Testing). In short, Beausang and Testing address different problems and resolve these problems in different ways.

Therefore, Applicants submit that Beausang and Testing are improperly combined. For completeness of response, Applicants now present reasons why, even if Beausang and Testing are

combinable, Claims 48 and 50 are neither disclosed nor suggested by this cited art.

Claim 48 Is Patentable Over The Cited References

Claim 48 recites:

> The memory model of Claim 47, wherein a plurality of tristate drivers can be coupled to the output ports of the memory out primitives, thereby representing an attribute of the read data port primitive.

Claim 48 depends from Claim 47 and therefore is patentable for at least the reasons presented for Claim 47. The Office Action cites the Abstract of Testing as disclosing the elements of Claim 48. Because neither Beausang nor Testing discloses a memory out primitive or a read data port primitive, they logically cannot disclose a further limitation regarding that a plurality of tristate drivers can be coupled to the output ports of the memory out primitives, thereby representing an attribute of the read data port primitive. Therefore, Applicants request reconsideration and withdrawal of the rejection of Claim 48.

Claim 50 Is Patentable Over The Cited References

Claim 50 recites:

> The memory model of Claim 49, wherein input ports of a plurality of tristate drivers can be coupled to output ports of the plurality of edge-triggered registers, thereby representing an attribute of the read data port primitive.

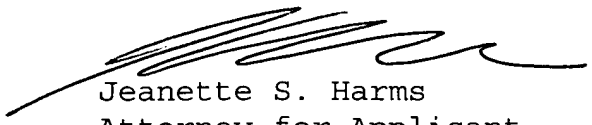
Claim 50 depends from Claim 49 and therefore is patentable for at least the reasons presented for Claim 49. The Office Action cites the Abstract of Testing as disclosing the elements of Claim 50. Because neither Beausang nor Testing discloses a read data port primitive, they logically cannot disclose a

further limitation that a plurality of tristate drivers can be coupled to the output ports of the plurality of edge-triggered registers, thereby representing an attribute of the read data port primitive. Therefore, Applicants request reconsideration and withdrawal of the rejection of Claim 50.

IX. CONCLUSION

For the foregoing reasons, it is submitted that the Examiner's rejections of Claims 37-53 and 55-58 are erroneous, and reversal of these rejections is respectfully requested.

Respectfully submitted,



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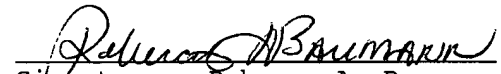
Signature: Rebecca A. Baumann

X. APPENDIX A

1-36 (Cancelled)

37. (Previously Presented) A memory model usable for simulation and automatic test pattern generation, the memory model comprising:

a memory primitive comprising a write_address port, a write_data port, and an output port;

a read data port primitive comprising a read_data port for coupling to the output port of the memory primitive, a read_address port, and an output port;

an address bus primitive comprising an output port for coupling to the write_address port of the memory primitive and the read_address port of the read data port primitive;

a data bus primitive comprising an output port for coupling to the write_data port of the memory primitive; and

a plurality of memory out primitives, each memory out primitive comprising an input port for coupling to the output port of the read data port primitive.

38. (Previously Presented) The memory model of Claim 37, wherein the memory primitive further includes:

a set input port;

a reset port;

a write_clock port; and

a write_enable port.

39. (Previously Presented) The memory model of Claim 37, wherein the read data port primitive represents a read port functionality of the memory.

40. (Previously Presented) The memory model of Claim 39, wherein a dimension of the output port of the read data port corresponds to a data dimension of the memory primitive.

41. (Previously Presented) The memory model of Claim 37, wherein the address bus primitive represents an address functionality of a memory.

42. (Previously Presented) The memory model of Claim 41, wherein the address bus primitive includes:

a plurality of input ports corresponding to an address dimension of the memory primitive.

43. (Previously Presented) The memory model of Claim 42, wherein the address bus primitive further includes an attribute indicating whether an incoming address is encoded or decoded.

44. (Previously Presented) The memory model of Claim 43, wherein the data bus primitive represents a data bus functionality of the memory.

45. (Previously Presented) The memory model of Claim 44, wherein the data bus includes:

a plurality of input ports corresponding to a data dimension of the memory primitive.

46. (Previously Presented) The memory model of Claim 37, wherein each memory out primitive represents a simulated value storage functionality of the memory.

47. (Previously Presented) The memory model of Claim 37, wherein each memory out primitive includes an output port.

48. (Previously Presented) The memory model of Claim 47, wherein a plurality of tristate drivers can be coupled to the output ports of the memory out primitives, thereby representing an attribute of the read data port primitive.

49. (Previously Presented) The memory model of Claim 47, wherein a plurality of edge-triggered registers can be coupled to the output ports of the memory out primitives, thereby representing an attribute of the read data port primitive.

50. (Previously Presented) The memory model of Claim 49, wherein input ports of a plurality of tristate drivers can be coupled to output ports of the plurality of edge-triggered registers, thereby representing an attribute of the read data port primitive.

51. (Previously Presented) A content addressable memory model usable for simulation and automatic test pattern generation, the content addressable memory model comprising:

a memory primitive including an output port;

a compare port primitive including a data port for coupling to the output port of the memory primitive, a data bus port, and an output port;

a data bus primitive including an output port for coupling to the data bus port of the compare port primitive;

a plurality of memory output primitives, each memory output primitive including an input port for coupling to the output port of the compare port primitive and an output port; and

an address bus primitive including input ports for coupling the output ports of a set of the memory output primitives.

52. (Previously Presented) The content addressable memory model of Claim 51, wherein the compare port primitive further includes:

a compare enable port for receiving a compare signal.

53. (Previously Presented) A combined content addressable memory (CAM) and random access memory (RAM) model usable for simulation and automatic test pattern generation, the combined CAM and RAM model comprising:

a first memory primitive including an output port;

a data bus primitive including an output port;

a compare port primitive for coupling to the memory primitive and the data bus primitive, the compare port primitive comprising;

a compare enable port;

a data bus port for coupling to the output port of the data bus primitive;

a data port for coupling to the output port of the first memory primitive; and

an output port;

a first plurality of memory output primitives, each memory output primitive including an output port and an input port for coupling to the output port of the compare port primitive;

an address bus primitive including an output port and input ports for coupling to output ports of a first subset of the first plurality of memory output primitives;

a second memory primitive including an output port;

a read data port primitive including a first input port for coupling to the output port of the second memory primitive, a second input port for coupling to an output port of the address bus primitive, and a third input port for coupling to the output

ports of a second subset of the plurality of memory output primitives; and

a second plurality of memory output primitives, each memory output primitive including an input port for coupling to an output port of the read data port primitive.

54. (Cancelled)

55. (Previously Presented) A memory model compatible with a simulation tool and an automatic test pattern generation (ATPG) tool, the memory model including:

a plurality of primitives, each primitive representing a defined functionality of a memory.

56. (Previously Presented) The memory model of Claim 55, wherein each primitive usable by the ATPG tool is configured based on a subset of behavioral hardware description language (HDL) usable by the simulation tool.

57. (Previously Presented) The memory model of Claim 56, wherein the behavioral HDL includes Verilog.

58. (Previously Presented) The memory model of Claim 56, wherein the subset of behavioral HDL can directly map to the plurality of primitives.